REMARKS

Upon entry of this amendment, which amends claims 1, 7-10, 15, 20, 21 and 26, claims 1-26 remain pending. In the June 19, 2002 Office Action, various objections were made to the disclosure and to the claims. Claims 1, 7-10, 15, 20 21 and 26 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 1-20 were rejected under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent No. 6,205,571 to Camporese et al. (hereinafter referred to as "Camporese") in view of U.S. Patent No. 6,305,001 to Graef (hereinafter referred to as "Graef"). Applicant respectfully requests reconsideration of the claims in view of the above amendments and the comments below.

Objections to the Disclosure

On page 2 of the June 19, 2002 Office Action, the specification was objected to for misspelling the words "assess" in line 18, at page 4 and "though" in line 6, at page 13. Additionally, the specification was objected to for not accurately stating that the combining of the simulations results in a complete clock net *simulation*.

In this Amendment, the specification has been amended to correct the misspellings and make clear that the result of combining the simulations is a complete clock net *simulation* and not the complete clock net itself. Applicant requests, therefore, that the objections to the disclosure be withdrawn.

Objections to the Claims

On pages 2-3 of the Office Action, claims 1, 7-10, 15, 20, 21 and 26 were objected to for not clarifying that combining the simulations form a "complete clock net simulation" rather than the "complete clock net" itself. In this Amendment, the claims have been amended so that it is

clear that combining the simulations forms a complete clock net *simulation*. Accordingly, Applicant requests that these objections to claims 1, 7-10, 15, 20, 21 and 26 be withdrawn.

Claims 7, 20 and 26 were also objected to for use of the words "assuming" and "assumes", as they purportedly "denote uncertainty". Applicant respectfully disagrees. There is nothing uncertain concerning use of these words in the context of the claimed invention. As explained in the detailed description of the invention, "each of the plurality of local clock nets would be simulated under the assumption that the clock arrival times from the global clock net would be simultaneous at all points where the local clock net is connected to the global clock net." (page 14, lines 9-11). This assumption simplifies the computational intensity of the simulation and, as explained in line 15 on page 13 of the specification, is an "assumption [that] is substantially accurate as this is the goal of the clock net designer." As explained later, and as is claimed in some of the dependent claims in the application, if the simulation of these assumed clock arrival times does not lead to convergence to the actual clock arrival times, the simulations and other steps in blocks 32-37 may be repeated using the calculated times rather than the assumed simultaneous times. (See, e.g., line 14, page 14 through line 6, page 15). Understanding this, Applicant respectfully believes that it cannot be properly said that the act of assuming simultaneous clock arrival times is uncertain. Nor can it be properly said that assuming the arrival times are simultaneous during the act of simulating leads to uncertainty (if that what the Examiner is suggesting). Even if it did in the latter case, Applicant believes that the objection would be improper. For the foregoing reasons, Applicant respectfully believes that the objections to claims 7, 20 and 26 cannot be properly maintained and, therefore, respectfully requests that they be withdrawn.

Claim 8 was also objected to for not indicated "where the simulated loads are being inserted". Claim 8 has been amended and no longer uses the word "inserting". Accordingly, the objection is now believed to be moot.

Claim 9 was also objected to for not being clear that the simulation of the complete clock net is evaluated and not the clock net itself. Claim 9 has been amended to overcome this objection. Accordingly, Applicant requests that the objection be withdrawn.

Finally, claim 26 was objected to for not using the gerund forms of the words "re-simulates" and "combines" in the claim. Applicant respectfully disagrees. A gerund is a verb form, ending in *-ing*, which acts as a noun in a sentence or phrase. The words "re-simulates" and "combines" are verbs, which describe the action performed by the "net simulator" and the "merging unit" elements in the claim. They are not meant to be nouns or take the form of gerunds in claim 26. Indeed, if the words "re-simulates" and "combines" were changed to their gerund forms, the actions performed by the "net simulator" and the "merging unit" elements of claim 26 would be absent and the claim would be rendered indefinite. Accordingly, Applicant respectfully believes that this objection to claim 26 is improper and requests that it be withdrawn.

Claim Rejections – 35 U.S.C. § 112, Second Paragraph

On page 2 of the Office Action, claims 1-26 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Specifically, claims 1, 10, 15, 20, 21 and 26 were rejected for not including all the information in the specification from which the simulation may be based. Applicant disagrees. Not including all characteristics of the exemplary embodiment described in the specification in claims 1, 10, 15, 20, 21 and 26 does not render any of them indefinite. Furthermore, there is no rule that requires that a claim include all characteristics or limitations of an embodiment

illustrated in the detailed description of the invention. The detailed description of the present invention clearly explains that the embodiments described in the detailed description section of the application are not intended to be limiting but, rather, illustrative. See the first paragraph on page 10 of the disclosure, which states:

> Embodiments of the present invention are described herein in the context of a unified database system to store, combine, and manipulate clock related data for a grid-based clock distribution design. *Those of ordinary skill in the art will realize that the following detailed description of the present invention is illustrative only and is not intended to be in any way limiting.* Other embodiments of the present invention will readily suggest themselves to such skilled persons having the benefit of this disclosure.

(emphasis supplied).

Applicant believes that grounds for setting forth the § 112 rejections of claims 1, 10, 15, 20, 21 and 26 are improper and, therefore, requests that the rejections be withdrawn.

Claims 8, 9 and 26 and each of their respective dependent claims were rejected for various instances of a lack of antecedent basis. Applicant has corrected all antecedent basis issues concerning these claims and requests, therefore, that the § 112 rejections of these claims be withdrawn.

Claim Rejections – 35 U.S.C. § 103(a)

On pages 3-10 of the Office Action, claims 1-20 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Camporese in view of Graef. For the following reasons Applicant respectfully disagrees.

A prior art reference or combination of references must teach each and every limitation of a claim in order to support a legitimate a § 103 rejection of the claim. (*See*, M.P.E.P. § 2143.) As explained in detail below, because Camporese in view of Graef does not teach and every

limitation of the presently claimed invention. Applicant respectfully believes that the § 103 rejections of claims 1-20 cannot be properly maintained.

Camporese discloses an X-Y grid tree clock distribution network for distributing a clock signal across a VLSI chip. Figure 2 of Camporese, in particular, shows a grid tree network where a buffer 200 receives and re-powers a clock signal and couples it to a first level tree wiring network 201, which then distributes the clock signal to a second level of tree wires 203 via re-powering buffers 202. The second level of tree wires 203 then distributes the clock signal to a number of points on the X-Y grid 204.

In column 6 of Camporese, the design and tuning of a clock distribution network is described. In lines 10-23, laying out an X-Y grid is described. In lines 24-43, selecting buffers and distributing them uniformly over the X-Y grid and to the wiring networks is described. In lines 44-47, it is mentioned how buffer placement, tree network and grid placement may be adjusted to take into account transistor level or wiring blockages. Finally, in lines 48-65, it is described how an electrical net list is created using a conventional extraction process and how a conventional transient simulation process can be performed.

Graef discloses a method of designing an integrated circuit (IC), which includes a method of planning a clock distribution network in the conceptual design phase of the IC. Figure 6 and the accompanying description in columns 8 and 9 describe the method of designing the IC. In step 100, a design specification for the IC is prepared. In step 110, a technology-independent description is produced. The technology-independent description consists of a functional description of the design and all of its subsystem elements that satisfy the IC design specification is prepared. In step 120, the technology-independent description is functionally partitioned into separate modules by consulting technology files containing packaging, I/O capabilities and other

technology-dependent information. Then, in step 125 a clock budgeting plan is created by partitioning the technology-independent description into separate, distinct groups based on the switching or clocking time of the recipients (e.g., flip-flops, registers, latches, etc.) in each of the partitioned groups. In other words, the technology-independent description is partitioned by clustering or grouping clock recipients which switch or clock at the same time such that the clock recipients in each of the target timing groups switch or clock at the same time while the clock recipients in different target timing groups switch at different times. (See, column 9, lines 18-35 of Graef.)

Independent claims 1, 15 and 21, by contrast, contain a number of characteristics that are not taught by Camporese in view of Graef.

First, independent claim 1 includes, among other steps, a step of "partitioning a complete clock net into a global clock net and a plurality of local clock nets". Similarly, independent claim 15 includes "means for partitioning a complete clock net into a global clock net and a plurality of local clock nets". Camporese, whether considered alone or combined with or modified by Graef, does not teach these elements of independent claims 1 and 15. Despite this, it is asserted in the Office Action that Figure 2 teaches the step of "partitioning" in claim 1. Applicant respectfully disagrees. While Figure 2 illustrates a clock distribution network, there is no teaching of "partitioning" it into a "global clock net" and a "plurality of local clock nets". In setting forth the rejection of claim 1, the Examiner has acted to "partition" the clock distribution network in Figure 2 on his own, designate what he believes are a global clock net and plurality of local clock nets and then claim that Camporese teaches these actions. Camporese simply does not teach or suggest such actions. It is also asserted in the Office Action that column 15, line 42 to column 17, line 4 of Graef teach the "means for partitioning a complete clock net into a global

clock net and a plurality of local clock nets" as recited in independent claim 15. Applicant disagrees. Line 42 of column 15 to line 4 of column 17 in Graef describe how the methods described in the patent may be practiced on a general purpose computer or in an ECAD system running on a general purpose computer. Details of the general purpose computer and different types of storage media are described in the cited portion of Graef. However, there is nothing in the cited portion that teaches or suggests the "means for partitioning..." element of claim 15. Accordingly, for at least this first reason, Applicant respectfully believes that Camporese in view of Graef cannot be properly maintained to support the § 103 rejections of independent claims 1 and 15.

Second, independent claim 1 includes, among other steps, a step of "simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net". Similarly, independent claim 15 includes "means for simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net". Camporese, whether considered alone or combined with or modified by Graef, does not teach these elements of independent claims 1 and 15. Despite this, it is asserted in the Office Action that lines 12-23 in column 12 of Camporese teach the step in claim 1 and that column 15, line 42 to column 17, line 4 teaches the element in claim 15. Applicant respectfully disagrees. Lines 12-23 in column 12 of Camporese describe how portions of some tree wiring levels may be removed by a "tree branch deletion method". However, there is nothing in that cited portion of Camporese that teaches or suggests simulating a local clock net, as recited in independent claims 1 and 15. Line 42 of column 15 to line 4 of column 17 in Graef describe how the methods described in the patent may be practiced on a general purpose computer or in an ECAD system running on a general purpose computer. Details of the general

purpose computer and different types of storage media are described in the cited portion of Graef. However, there is nothing in the cited portion of Graef that teaches or suggests the "means for simulating each of the plurality of local clock nets to generate a load..." element recited in claim 15. Accordingly, for at least this second reason, Applicant respectfully believes that Camporese in view of Graef cannot be properly maintained to support the § 103 rejections of independent claims 1 and 15.

Third, independent claim 1 includes, among other steps, a step of "simulating the global clock net based on the simulated load of each of the plurality of local clock nets". Similarly, independent claim 15 includes "means for simulating the global clock net based in part on the simulated load of each of the plurality of clock nets". Camporese, whether considered alone or combined with or modified by Graef, does not teach these elements of independent claims 1 and 15. Despite this, it is asserted in the Office Action that lines 12-23 in column 12 of Camporese teach the step in claim 1 and that column 15, line 42 to column 17, line 4 teaches the element in claim 15. As explained above, lines 12-23 in column 12 of Camporese describe how portions of some tree wiring levels may be removed by a "tree branch deletion method". There is nothing in this cited portion of Camporese, however, that teaches or suggests a step of "simulating the global clock net..." as recited in independent claim 1. Also explained above was that line 42 of column 15 to line 4 of column 17 in Graef describe how the methods described in the patent may be practiced on a general purpose computer or in an ECAD system running on a general purpose computer. Details of the general purpose computer and different types of storage media are also described in the cited portion of Graef. However, there is nothing in the cited portion that teaches or suggests the "means for simulating the global clock net based in part on the simulated load of each of the plurality of clock nets" element recited in claim 15. Accordingly, for at least

this third reason, Applicant respectfully believes that Camporese in view of Graef cannot be properly maintained to support the § 103 rejections of independent claims 1 and 15.

Finally, independent claim 1 includes, among other steps, a step of "storing the plurality of simulations in the Clock Data Model". Similarly, independent claim 15 includes "means for storing the plurality of simulations". As described above Camporese, whether considered alone or combined with or modified by Graef, does not teach or suggest methods or apparatus for simulating a plurality of local clock nets. Because there is no teaching or suggestion of this simulation, these references cannot teach or suggest "storing the plurality of simulations" as recited in independent claims 1 and 15. Accordingly, for at least this fourth reason, Applicant respectfully believes that Camporese in view of Graef cannot be properly maintained to support the § 103 rejections of independent claims 1 and 15.

The above demonstrates that at least four of the elements of independent claims 1 and 15 are not taught or suggested by Camporese in view of Graef. Accordingly, Applicant believes that the § 103 rejections of independent claims 1 and 15 cannot be properly maintained and respectfully requests that they be withdrawn.

Claims 2-14 and 16-21 depend from independent claims 1 and 15, respectively. Accordingly, they are believed to be allowable over the cited prior art for the same reasons set forth above. Applicant requests, therefore, that the § 103 rejections of these claims also be withdrawn.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 408-282-1857.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning at line 2 on page 8 of the application has been amended as follows:

--A method of and an apparatus for determining clock insertion delays for a microprocessor design having a grid-based clock distribution is disclosed. The method includes partitioning the complete clock net into a global clock net and a plurality of local clock nets, simulating a load for each of the local clock nets, simulating the global clock net, and combining the simulations to form ~~the~~ a complete clock net simulation. The method may further include evaluating the combination to determine whether the results converge and storing the simulation results in a Clock Data Model. When the results do not converge, the method re-simulates at least one of the local clock nets and re-simulates the global clock net. The Clock Data Model collects, manages, retrieves, and queries all of the simulation information. The method may further analyze the complete clock net to predict the clock skew for a given data transfer path for potential redesign.--

The paragraph beginning at line 4 on page 11 of the application has been amended as follows:

--Turning now to FIG. 6, a logic flow diagram of a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution is shown. The method uses as an input a database containing the entire network information for the microprocessor. This includes the complete clock net information. Typically, the method extracts each piece of information from this database only once but this may not necessarily be the case. The process

begins at START. At block 30, the process partitions the complete clock net into a global clock net and a plurality of local clock nets. The global clock net includes levels ten through three and those portions of level two that are outside of all of the plurality of local clock nets. Each of the plurality of local clock nets includes portions of level two and level one. The location of the local clock nets can be determined in any of a number of ways. One valid approach is to break the complete clock net into a plurality of parts approximating rectangular grid coordinates. The designation of the global clock net may be thought of as horizontal partitioning. The designation of local clock nets may be thought of as vertical partitioning. It may be desired or required to break one or more of the local clock nets down even further. This would result in sub-, sub-sub-, etc. local clock nets. At block 32, the process simulates each of the plurality of local clock nets. The process will be described in more detail below. If sub-local clock nets were created in block 30, then the lowest sub-local clock net is simulated first and then each successively higher sub-local clock net is simulated until the highest local clock net has been simulated. In those instances when the simulations of the local clock nets do not depend on one another, they may be processed in parallel. The result is a load for each of the local clock nets on the global clock net. This load may take many forms. One valid form is that of a single capacitor for each of the connections of the local clock net to the global clock net. At block 34, the process simulates the global clock net based in part on the simulated load of each of the plurality of local clock nets. This will also be described in more detail below. At block 36, the process combines the simulations to form ~~the~~ a complete clock net simulation. At decision block 37, the complete clock net is evaluated to determine if the results converge. It is possible, if somewhat unlikely, that this block could be eliminated. Often, the results of the first pass will not converge as one would prefer and blocks 32 through 37 will be repeated at least once if not more. More details of

this iteration aspect of the method will be described below.--

The paragraph beginning at line 8 on page 14 of the application has been amended as follows:

--Returning to FIG. 6, taken together, blocks 32-36 and the blocks of FIGsS. 7 and 8 result in the initial set up of the CDM. Recall that in FIG. 7 each of the plurality of local clock nets was simulated under the assumption that the clock arrival times from the global clock net would be simultaneous at all points where the local clock net is connected to the global clock net. Recall further that these times were subsequently calculated in block 34 and FIG. 8. As a result, the assumed clock arrival value and the actual clock arrival value can be compared in block 37. If the values have not converged, then blocks 32-37 can be repeated using the calculated times rather than the assumed simultaneous times in block 42 of FIG. 7. Such an iteration will improve the accuracy of the simulations. Although the entirety of blocks 32-37 and the corresponding blocks of FIGsS. 7 and 8 may be repeated, this may be undesirable and unnecessary. A more streamlined approach would be to asses each of the plurality of local clock nets in a top down manner to determine whether to re-run the simulation for each particular local clock net. Similar to above, the simulations may be re-run in parallel. All of the local clock nets are reviewed and re-run in block 32 before the global clock net is re-run in block 34. It may not be necessary to re-run the global clock net simulation if the re-calculated loads of the local clock nets attached directly to the global clock net have not changed substantially, that is, they have not changed enough to affect the clock arrival times of the global clock net. As the various simulations are re-run, the CDM is updated. In an effort to further streamline the iteration process, it is possible to skip blocks 38 and 40 of FIG. 7 as this information is already stored in the CDM and has not changed. Also, it is possible to skip blocks 46 and 48 of FIG. 8 for the

same reason. Eventually through the iteration process the results will converge and the process will end leaving a substantially fully developed simulation and CDM.--

IN THE CLAIMS:

Claims 1, 7-10, 15, 20, 21 and 26 have been amended as follows:

1. (Once Amended) A Clock Data Model (CDM) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising:

partitioning ~~the~~a complete clock net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

combining the plurality of simulations to form ~~the~~a complete clock net simulation; and

storing the plurality of simulations in the Clock Data Model.

7. (Once Amended) The CDM as defined in claim 6, wherein ~~simulating the local clock net comprises assuming that the~~ clock arrival times from the global clock net ~~will be simultaneous~~ at all points where ~~the~~a given local clock net is connected to the global clock net are assumed to occur simultaneously when the given local clock net is being simulated.

8. (Once Amended) The CDM as defined in claim 1, wherein simulating the global clock net comprises:

extracting the layout of the global clock net from a microprocessor network database;

extracting component values of the elements of the global clock net from the microprocessor network database;

~~inserting~~extracting the simulated loads of the plurality of local clock nets from the CDM; and

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads.

9. (Once Amended) The CDM as defined in claim 1, wherein the method further comprises evaluating the complete clock net simulation to determine whether ~~the~~ results of the simulations converge.

10. (Once Amended) The CDM as defined in claim 9, wherein, if the results do not converge, the method further comprises:

~~assuming that clock arrival times are those calculated for the simulated global clock net;~~

re-simulating the at least one of the plurality of local clock nets using a corresponding calculated clock arrival time, to generate a load for the at least one local clock net on the global clock net;

re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets; and

combining the simulations and re-simulations to form the complete clock net simulation.

15. (Once Amended) A Clock Data Model (CDM) for use with a system for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the system comprising means for partitioning ~~the~~a complete clock net into a global clock net and a plurality of local clock nets, means for simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, means for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets, and means for combining the plurality of simulations to form ~~the~~ a complete clock net simulation, the CDM comprising:

means for storing the plurality of simulation results.

20. (Once Amended) The CDM as defined in claim 15, wherein the system further comprises means for evaluating the complete clock net to determine whether the results converge, means for assuming that clock arrival times are those calculated for the simulated global clock net, means for re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, means for re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets, and means for combining the simulations and re-simulations to form the complete clock net simulation and wherein the CDM further comprises means for storing the plurality of re-simulation results.

21. (Once Amended) A Clock Data Model (CDM) for use with a system for determining clock insertion delays for a microprocessor design having grid-based clock

distribution, the system comprising a partitioner for horizontally and vertically partitioning ~~the~~a complete clock net into a global clock net and a plurality of local clock nets, at least one local clock net simulator for simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, a global clock net simulator for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets, and a merging unit for combining the plurality of simulations to form ~~the~~a complete clock net simulation, the CDM comprising:

a memory for storing the plurality of simulation results.

26. (Once Amended) The CDM as defined in claim 21, wherein the system further comprises a convergence evaluator for evaluating the complete clock net to determine whether the results converge and, when the results are found not to converge, the ~~apparatus~~system assumes that clock arrival times are those calculated for the simulated global clock net, the at least one local clock net simulator re-simulates at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, the global clock net simulator re-simulates the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets, and the merging unit combines the simulations and re-simulations to form the complete clock net simulation and wherein the CDM further comprises a memory for storing the plurality of re-simulation results.